REMARKS

Reconsideration of the above-identified application in view of the following is respectfully requested.

Claim 29 has been amended to correct a minor informality.

Claims 26-32 have been rejected as anticipated by Bishop, US 4,393,492.

Claim 26 recites a first communications section being arranged to respond to reception of a clock transition signal along a first communications link by transmitting a clock transition signal having the same polarity back along the first communications link and a second communications section being arranged to respond to reception of a clock transition signal along a second communications link by transmitting a clock transition signal having the opposite polarity back along the second communications link. The Office Action states that Bishop discloses a "device having at least first and second communication sections suitable for connection to similar devices along different bidirectional communication links [Bishop, a central office 12, subscriber terminal 14, and drop terminal 16, Fig. 1]" (Office Action, page 2).

Bishop discloses a central office 12 connected to both a subscriber terminal 14 and a drop terminal 16 by a single bidirectional communications link formed by an outgoing line 18 and an incoming line 20 (Fig. 1). Thus, Bishop does not disclose a device having at least first and second communications sections suitable for connection to similar devices along different bidirectional communication links, as recited by claim 26.

Further, the Office Action states that Bishop, Col. 35, lines 40-60 discloses a first communications section arranged to respond to reception of a clock transition signal along a first communications link by transmitting a clock transition signal having the same polarity back along the first communications link and a second communications section arranged to respond to reception of a clock transmission signal along a second communications link by transmitting a clock transmission signal having the opposite polarity back along the second communications link.

As discussed above, Bishop discloses only a single bidirectional communications link (formed by outgoing line 18 and incoming line 20) connecting the central office 12 to both of the subscriber terminal 14 and a drop terminal 16. It is respectfully submitted that Bishop does not reasonably suggest in any way that the central office 12 of Fig. 1 can have two communication sections connected to two respective communications links and arranged to respond differently to signals received along the two different links. Col. 35, lines 40-60 of Bishop do not disclose, either expressly or inherently, these features.

Bishop, Col. 35, lines 40-60, discloses the operation of a remote alarm decoder circuit 256 of the central office 12. A least significant bit (LSB) of frame 1 of the signal sent to a destination terminal can be used to confirm receipt of the signal by the destination terminal (Bishop, Col. 35, lines 40-60). In Bishop, all of the signals from the central office 12 for all terminals (such as the subscriber terminal 14 and the drop terminal 16) are sent along outgoing line 18. The signals are received and forwarded in turn by the terminals and eventually returned to the central office along the incoming line 20 (Fig. 1). Each destination terminal of Bishop includes circuitry

which responds to receipt of signals intended for that terminal by reversing the polarity of the least significant bit of frame 1 of the received signal before the signal is sent back to the central office along the incoming line 20.

Bishop, Col. 35, line 62, to Col. 36, line 10 explains that if a signal is returned to the central office 12 without the polarity of the least significant bit of frame 1 being changed, an alarm is generated indicating that this signal has not been received at the intended destination terminal. It is respectfully submitted that the technique disclosed in Bishop of using a polarity change of a specific bit of a signal as a flag to confirm successful receipt is not the same as recited in claim 26.

In communications systems, clock signals to control and synchronize the timing of operations carried out at different parts of the system and the data transmitted by the communication system are used for different purposes and are responded to in entirely different ways. Accordingly, although Bishop does disclose reversing the polarity of one bit of a received signal before returning the signal, this technique is the polarity reversal of one bit of transmitted data to act as a flag confirming successful receipt of the signal, not a clock signal.

Thus, Bishop discloses a communications system in which each terminal responds to receipt of signals directed to itself by reversing the polarity of one bit of the signal to act as a "confirmation of receipt" flag and re-transmitting the signal back to the central office 12. Thus, in Bishop, the reversal of the polarity of the specified bit of the received signal before re-transmission must always be carried out in order for the polarity of the bit in the returned signal to be useful as an indication to the central office 12 whether the destination terminal received the signal.

Accordingly, the requirement of Bishop that the polarity of one bit of the received signal must always be reversed before the signal is returned, to confirm receipt, would not have suggested to one of ordinary skill in the art first and second communications sections connected along different bi-directional communications links with the first communication section able to respond to reception of a clock transition signal along a first communications link by transmitting a clock transition signal having the same polarity back along the first communications link and the second communications section able to respond to reception of a clock transition signal along a second communications link by transmitting a clock transition signal having the opposite polarity back along the second communications link, as recited in claim 26. Thus, claim 26 is allowable.

Claim 27 recites that the first communications section holds a first clock logic level and an output, when the first communications section is not connected to another device, and the second communications section holds a second clock logic level having an opposite polarity to the first clock state logic level as an input, when the second communications section is not connected to another device. Claim 28 recites the second communications section holds a first clock logic level as an output, when the second communications section is not connected to another device, and the first communications section holds a second clock logic level having an opposite polarity to the first clock state logic level as an output, when the first communications section is not connected to another device.

The Office Action, page 3, cites the stored low level signal of Bishop, Col. 15, line 65, for these features. Bishop, Col. 15, lines 64-67 , discloses the operation of a

gate 86 (Fig. 4B). The gate 86 is an exclusive OR gate which generates a low level output signal when its two inputs are the same and a high level output when its two inputs are different. Col. 15, lines 64-67 and Col. 16, lines 6-10 only disclose that the gate 86 generates a low level when its two inputs are the same. However, one of ordinary skill in the art would discern that an exclusive OR gate generating a low level output when its inputs are the same will generate a high level output when its inputs are different.

It is respectfully submitted that the operation of the exclusive OR gate 86 of Bishop would not have been regarded, by one of ordinary skill in the art, as the features of claims 27 and 28 defining first and second communication sections which are each suitable for connection to other devices along different bidirectional communications links. The single exclusive OR logic gate 86 of Bishop is not capable of being connected to a bidirectional communication link.

Further, claims 27 and 28 specify inter-relationships between the input and output signals held by first and second communication sections of the device when the first and second communication sections are not connected to another device. Such inter-relationships between the input and output logic levels of two different communication sections is not disclosed by the single logic gate 86 of Bishop because it is not possible for a single gate to disclose a relationship between two different devices. Therefore, claims 27 and 28 are allowable.

Claim 29 recites that the linked communication sections form a loop, when the first communications section is linked to the second communications section of another device or vice-versa through a bi-directional communications link, and that

the device uses an oscillating clock transition signal passing around the loop as a clock signal for communication along the communications link. The Office Action, page 4, cites the loopback circuit of Bishop, Col. 29, line 48 for these features.

The loopback circuit 24 of Bishop allows signals returning to the central office 12 along the incoming line 20 to be selectively directed back onto the outgoing line 18 so that they are resent to the subscriber terminal 14. Bishop, Col. 29, lines 34-47 discloses that the loopback circuit 24 identifies signals containing errors indicating that they have not been properly received by the subscriber terminal 14 and, if such errors are detected, the signal is selectively passed to the outgoing line 18 so that it is returned to the subscriber terminal 14, giving a second opportunity for the signal to be properly received.

Such selective looping of improperly received signals to allow a further opportunity for receiving is not an oscillating clock transition signal passing around a loop and does not in any way suggest a device using such oscillating clock transition signals as a clock signal for communication along a communications link, as recited by claim 29. Therefore, claim 29 is allowable.

Claim 30 recites that, when the first and second communication sections are first linked, the difference between their held input and output clock logic levels causes the oscillating clock transition signals to begin passing around the loop. The Office Action, page 4, cites the loopback circuit of Bishop, Col. 29, line 48 for these features.

The loopback circuit 24 of Bishop, as explained above, selectively reroutes improperly received signals. Bishop does not disclose an oscillating clock transition

signal passing around a loop. Thus, Bishop does not disclose first and second communication sections having held input and output clock logic levels which cause oscillating clock transition signals to begin passing around a loop when they are first linked, as recited by claim 30. Therefore, claim 30 is allowable.

Claim 31 recites a loop formed by a first device receiving a clock transition signal along a communications link and sending a clock transition signal having the same polarity back along the communications link and a second device receiving a clock transition signal along a communications link and sending a clock transition signal having the opposite polarity back along the communications link. The first and second devices use the oscillating clock transition signals traveling around the loop to provide a clock signal to control data transfer along the communications link. The Office Action cites Bishop, Fig. 1 & Col. 35, lines 40-60, for these features.

As explained above, Bishop in particular the circuit shown in Fig. 1, does not disclose these features, as recited by claim 31. Bishop in no way suggests a clock transition signal. As explained above, although Bishop does disclose a system including signals traveling around a loop, the signals traveling around the loop are data signals which are selectively routed around the loop by the loopback circuit 24, if they have not been properly received by a subscriber terminal 14. Bishop does not disclose that the signals passing round the loop are used as clock signals to control data transfer along a bidirectional communications link. Further, it would be impossible for the signals of Bishop to be used in this manner. Thus, claim 31 is allowable.

Claim 32 recites that the clock transition signals traveling around the loop are used as the clock signal. The Office Action cites Bishop, Col. 29, line 48 for this feature. As stated above, Bishop does not disclose this feature. It would be impossible to use the signals routed by the loopback circuit 24 of Bishop as clock signals since, as explained in Bishop, Col. 29, lines 11-47, the loopback circuit 24 selectively transfers signals from the incoming line 20 back to the outgoing line 18 so that they are looped back to a subscriber terminal 14 only when errors are identified in the signal thereby indicating that the signal was not properly received by the subscriber terminal 14. Where the signals have been properly received by a subscriber terminal 14 so that they do not include errors, the loopback circuit 24 allows the signals to continue along the ingoing line and does not loop them back. Thus, the passing of signals around the loop by the loopback circuit 24 of Bishop is dependent upon failure to properly receive the signal at a subscriber terminal 14. Thus, it cannot be predicted in advance whether a specific signal will or will not be passed around the loop by the loopback circuit 24. This unpredictability precludes signals of the loopback circuit 24 of Bishop as timing signals.

Consequently, claims 26 and 31, as well as claims 27-30 and 32 which depend from claims 26 and 31, respectively, are in condition for allowance. In view of the foregoing, it is respectfully requested that the amendment be entered and the application allowed.

Please charge any deficiency or credit any overpayment in the fees for this amendment to our Deposit Account No. 20-0090.

Respectfully submitted,

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